## IN THE CLAIMS

The status of the claims is noted below.

- 1. (Currently Amended) Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal  $(m_d(t))$ , a stereo-sum signal  $(m_s(t))$  and a pilot carrier, comprising a PLL-circuit to recover the pilot carrier and/or or at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives the sampling rate decimated stereo-sum signal  $(m_s(t))$  as input signal, which is sampling rate decimated by a decimation factor of D.
- 2. (Previously Presented) Stereo demultiplexer according to claim 1, wherein said sampling rate decimated stereo-sum signal  $(m_s(t))$  is further sampling rate decimated by a decimation factor of E before said PLL-circuit receives it as input signal.
- 3. (Currently Amended) Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal  $(m_d(t))$ , a stereo-sum signal  $(m_s(t))$  and a pilot carrier, comprising a PLL-circuit to recover the pilot carrier and/or or at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives the sampling rate decimated stereo-sum signal  $(m_s(t))$  as input signal, which is sampling rate decimated by a decimation factor of D,

wherein said PLL-circuit outputs a recovered pilot carrier which is interpolated so that it has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.

- 4 (Previously Presented) Stereo demultiplexer according to claim 3, wherein that D-1 or  $(E \cdot D)$ -1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) and one calculated pilot carrier value (y(k/D)) are alternately output.
- 5. (Previously Presented) Stereo demultiplexer according to claim 4, wherein said interpolation within the PLL-circuit is performed on basis of a prediction starting at said calculated pilot carrier value.
  - 6. (Previously Presented) Stereo demultiplexer according to claim 5, including
  - a PLL within the PLL-circuit which outputs a phase signal, and
- a first sine calculation unit which outputs said one calculated pilot carrier value (y(k/D)) on the basis of said phase signal.

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- 7. (Previously Presented) Stereo demultiplexer according to claim 6, including
- second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation units each of which outputs one of said D-1 or  $(E \cdot D)$ -1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) on basis of said phase signal and a respective added phase shift value.
  - 8. (Currently Amended) Stereo demultiplexer according to claim 6, including
- a third multiplexer which multiplies said phase signal with a factor of 2 before it is input to said first sine calculation unit  $\frac{\text{and/or or}}{\text{or}}$  a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation unit via a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  adder which adds said respective phase shift value so that the  $2^{nd}$  harmonic of the pilot carrier is generated.
- 9. (Previously Presented) Stereo demultiplexer according to claim 6, wherein said PLL comprises
- a first multiplier receiving samples of the stereo-sum signal (x(k)) as multiplicant at a first input,
  - a filter receiving the output signal of said first multiplier,
- a second multiplier multiplying said output signal of said filter with a PLL gain (PLL loop gain),
- a first adder receiving said output signal of said second multiplier at a first input as a first summand, a constant representing the product of the pilot carrier frequency ( $\omega_{pil}$ ) and the sampling period at a second input as a second summand, and a delayed phase signal which is the output signal of said first adder at a third input as a third summand,
- a delay element receiving said phase signal of said first adder and supplying said delayed phase signal to said third input of said first adder, and
- a cosine calculation unit receiving the phase signal of said first adder and supplying its output signal as multiplier to a second input of said first multiplier.

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- 10. (New) Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal (m<sub>d</sub>(t)), a stereo-sum signal (m<sub>s</sub>(t)) and a pilot carrier, comprising a PLL-circuit to recover the pilot carrier and at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives the sampling rate decimated stereo-sum signal (m<sub>s</sub>(t)) as input signal, which is sampling rate decimated by a decimation factor of D.
- 11. (New) Stereo demultiplexer according to claim 10, wherein said sampling rate decimated stereo-sum signal (m<sub>s</sub>(t)) is further sampling rate decimated by a decimation factor of E before said PLL-circuit receives it as input signal.
- 12. (New) Stereo demultiplexer receiving a frequency demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal ( $m_d(t)$ ), a stereo-sum signal ( $m_s(t)$ ) and a pilot carrier, comprising a PLL-circuit to recover the pilot carrier and at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives the sampling rate decimated stereo-sum signal ( $m_s(t)$ ) as input signal, which is sampling rate decimated by a decimation factor of D,

wherein said PLL-circuit outputs a recovered pilot carrier which is interpolated so that it has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.

- 13. (New) Stereo demultiplexer according to claim 12, wherein that D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) and one calculated pilot carrier value (y(k/D)) are alternately output.
- 14. (New) Stereo demultiplexer according to claim 13, wherein said interpolation within the PLL-circuit is performed on basis of a prediction starting at said calculated pilot carrier value.
  - 15. (New) Stereo demultiplexer according to claim 14, including
  - a PLL within the PLL-circuit which outputs a phase signal, and
- a first sine calculation unit which outputs said one calculated pilot carrier value (y(k/D)) on the basis of said phase signal.
  - 16. (New) Stereo demultiplexer according to claim 15, including

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- second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation units each of which outputs one of said D-1 or  $(E \cdot D)$ -1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) on basis of said phase signal and a respective added phase shift value.

## 17. (New) Stereo demultiplexer according to claim 15, including

- a third multiplexer which multiplies said phase signal with a factor of 2 before it is input to said first sine calculation unit and a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation unit via a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  adder which adds said respective phase shift value so that the  $2^{nd}$  harmonic of the pilot carrier is generated.

## 18. (New) Stereo demultiplexer according to claim 15, including

- a third multiplexer which multiplies said phase signal with a factor of 2 before it is input to said first sine calculation unit or a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation unit via a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  adder which adds said respective phase shift value so that the  $2^{nd}$  harmonic of the pilot carrier is generated.
  - 19. (New) Stereo demultiplexer according to claim 15, wherein said PLL comprises
- a first multiplier receiving samples of the stereo-sum signal (x(k)) as multiplicant at a first input,
  - a filter receiving the output signal of said first multiplier,
- a second multiplier multiplying said output signal of said filter with a PLL gain (PLL loop gain),
- a first adder receiving said output signal of said second multiplier at a first input as a first summand, a constant representing the product of the pilot carrier frequency ( $\omega_{pil}$ ) and the sampling period at a second input as a second summand, and a delayed phase signal which is the output signal of said first adder at a third input as a third summand,
- a delay element receiving said phase signal of said first adder and supplying said delayed phase signal to said third input of said first adder, and
- a cosine calculation unit receiving the phase signal of said first adder and supplying its output signal as multiplier to a second input of said first multiplier.

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- 20. (New) Stereo demultiplexer according to claim 6, including
- a third multiplexer which multiplies said phase signal with a factor of 2 before it is input to said first sine calculation unit and a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  sine calculation unit via a respective second to  $D^{th}$  or  $(E \cdot D)^{th}$  adder which adds said respective phase shift value so that the  $2^{nd}$  harmonic of the pilot carrier is generated.

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